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| APPLICATION NO.   | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.  | CONFIRMATION NO. |
|---|-------------|----------------------|----------------------|------------------|
| 09/578,511  | 05/26/2000  | Won Hyoung Park      | HI-004               | 7993             |
| 34610   | 7590        | 05/24/2005           | EXAMINER             |                  |
| FLESHNER & KIM, LLP<br>P.O. BOX 221200<br>CHANTILLY, VA 20153 |             |                      | GHULAMALI, QUTBUDDIN |                  |
|   |             |                      | ART UNIT             | PAPER NUMBER     |
|   |             |                      | 2637                 |                  |

DATE MAILED: 05/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

|                              |                 |  |                  |  |
|------------------------------|-----------------|--|------------------|--|
| <b>Office Action Summary</b> | Application No. |  | Applicant(s)     |  |
|                              | 09/578,511      |  | PARK, WON HYOUNG |  |
|                              | Examiner        |  | Art Unit         |  |
|                              | Qutub Ghulamali |  | 2637             |  |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12 November 2004.
- 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-17, 19-23, 25-33 and 35-42 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-5, 21 and 42 is/are allowed.
- 6) ☒ Claim(s) 6, 9-14, 19, 20, 22, 23, 25-29, 32, 33 and 35-39 is/are rejected.
- 7) ☒ Claim(s) 7, 8, 15-17, 30, 31, 40 and 41 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)             | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Acknowledgment*

1. This Office Action is responsive to the Amendment filed on 11/12/2004.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 6, 9-14, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Chalmers (US Patent 5,640,416).

Regarding claim 6, Chalmers discloses a digital sampler to sample an intermediate frequency signal (214, 416) (col. 4, lines 60-67; col. 7, lines 1-6);  
a zero-order holder (401) to determine amplitude of the sampled intermediate frequency signal (col. 7, lines 6-41);  
a quantizer to convert the sampled intermediate frequency signal processed by the zero-order holder to a digital signal (col. 5, lines 43-50);  
a plurality of latches (615, 617, 619, 621) to transmit the digital signal to a plurality of channels after a prescribed time delay (col. 16, lines 20-48); and

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a plurality of output formatters to periodically output the latched digital signal transmitted to corresponding channels of the plurality of channels (see col. 16, lines 40-48).

Regarding claim 9, Chalmers discloses the plurality of channels comprise an I and a Q channel (col. 16, lines 49-60).

Regarding claim 10, Chalmers discloses a signal processor, comprising a digitizer, which receives an analog signal and generates a digital signal, wherein the digitizer comprises:

a sampler, which receives and samples the analog signal (214, 416) (col. 4, lines 60-67; col. 7, lines 1-6);

a zero order hold (401) circuit, which receives an output of the sampler and determines an amplitude of the received signal, and

a quantizer, which receives an amount of the zero order hold circuit and generates the digital signal (col. 5, lines 43-50);

a channel separator, which receives the digital signal from the digitizer and separates the digital signal into at least 2 channels, each channel having a different phase (early, late) (col. 8, lines 61-67; col. 9, lines 1-12); and

a phase shift controller (501), which receives a clock signal and controls the phase shifting of the channel separator (col. 8, lines 49-60).

Regarding claim 11, Chalmers discloses channels comprise a Q channel and an I channel having a phase difference of approximately 90 degrees (see col. 16, lines 49-60).

Regarding claim 12, Chalmers discloses analog signal is an intermediate frequency CDMA formatted signal (col. 1, lines 15-28).

Regarding claim 13, Chalmers discloses an amount of the signal processor is a QPSK modulated digital signal, having a first component (I) and a second component (Q) out of phase with the first component (col. 16, lines 49-60).

Regarding claim 14, Chalmers discloses:  
a latch circuit which receives the digital signal and outputs a first signal and a second signal, wherein the second signal is a delayed first signal (col. 16, lines 20-48);  
an output formatted, which receives the first and second signals (I and Q) and outputs the first and second signals at prescribed periods (see col. 16, lines 40-48, 49-60).

Regarding claim 19, Chalmers discloses a plurality of buffers to receive and forward the clock signal (see col. 13, lines 18-20); and  
a logic circuit responsive to a buffered clock signal to generate a control signal to control an amount of the channel separator (see col. 13, lines 18-36).

Regarding claim 20, Chalmers discloses a plurality of Finite Impulse Response (FIR) filters coupled to receive an output of the channel separator, wherein an individual FIR filter is coupled to each channel of the at least two channels (see col. 4, lines 35-39, 60-67; col. 10, lines 58-67).

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 22, 23, 25-29, 32-33, and 35-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chalmers (US Patent 5,640,416).

Regarding claims 22, 23, 25-29, 32, 33, 35-39, Chalmers (figs. 3, 4, 5a), discloses an Analog-to-Digital converter (406) convert an intermediate frequency signal (214, 416) (aliased spectrum, see note below) into digital (digitized) signal (col. 4, lines 60-67), the digitized output from the A/D converter separates (308) and provides an In-phase (310) component and a quadrature (312) component of the digital signal (col. 7, lines 41-64), a plurality of filters (304,501) to filter the digital components in a polyphase low pass filter, outputs a complex corrected signal (col. 18, lines 45-59) using Code Division Multiple Access (CDMA) techniques. Chalmers fails to disclose providing a quadrature and an in-phase component of the digital signal. However, Chalmers shows at the output of the A/D converter the digitized signal separates (308) and provides an In-phase (310) component and a quadrature (312) component of the digital signal (col. 7, lines 41-64).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the separated digital components (first and second digital signals) outputted at the A/D converter device in such a way (in a single chip) so as to provide similarity of function (I and Q complex signal separation) as taught by Chalmers.

**NOTE:** By definition cited in “Technical Terms” second Edition by Daniel N. Lapedes, the aliasing is an “Introduction of error into the computed amplitudes of the lower frequencies in a Fourier analysis of a function carried out using discrete time samplings whose interval does not allow the proper analysis of the higher frequencies present in the analyzed function”.

***Allowable Subject Matter***

6. Claims 1-5, 21 and 42 allowed.
7. Claims 7, 8, 15-17, 30, 31, 40 and 41, are objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including *all of the limitations of the base claims* and *any intervening claims*.

***Conclusion***

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutub Ghulamali whose telephone number is (571) 272-3014. The examiner can normally be reached on Monday-Friday from 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QG.  
May 17, 2005.



**JAY K. PATEL**  
**SUPERVISORY PATENT EXAMINER**